

**REMARKS**

Claims 34-52 are pending in the present application. Claims 34 and 37-44 have been amended. Claims 45-52 have been presented herewith. Claims 22-33 have been canceled.

**Priority Under 35 U.S.C. 119**

Applicants note the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copies of the priority documents in parent application Serial No. 09/460,984.

**Claim Objections**

Claims 34 and 40 have been objected to in view of the informalities stated on page 2 of the current Office Action dated July 14, 2004. In view of the claim amendments, line 8 of claim 34 does not feature "the plurality of bumps". In claim 40, the ball bumps have antecedent in view of the ball bumps featured in claim 39. The Examiner is therefore respectfully requested to withdraw the objection to claims 34 and 40 for at least the above reasons.

**Claim Rejections-35 U.S.C. 103**

Claims 34-44 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Egawa reference (U.S. Patent No. 6,229,215) in view of the Imasu et al.

reference (U.S. Patent No. 6,208,525). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 34 includes in combination a BGA (ball grid array) type semiconductor device and a CSP (chip size packaged) type semiconductor device, the CSP type semiconductor device "having a semiconductor element which has main and back surfaces, and side surfaces between the main and back surfaces, and a plurality of terminals which are formed on the main surface, wherein the back surface and the entirety of the side surfaces of the semiconductor element are exposed". Applicants respectfully submit that the semiconductor device of claim 34 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has interpreted second semiconductor chip 17 in Fig. 1(b) of the Egawa reference as the CSP type semiconductor device of claim 34. However, as may be readily understood in view of Fig. 1(b) of the Egawa reference, resin 19 covers side surfaces of second semiconductor chip 17, contrary to the features in claim 34. Similarly, semiconductor chip 10 in Fig. 11 of the Imasu et al. reference has adhesive 16 on side surfaces thereof, contrary to the features of claim 34. Since the side surfaces of the semiconductor chips in the relied upon prior art interpreted as the CSP type semiconductor device of claim 34 are not exposed, the prior art structures do not achieve a higher level of heat discharge performance as the semiconductor device of claim 34. Applicants therefore respectfully submit that the semiconductor device of

claim 34 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 34-38, is improper for at least these reasons.

The semiconductor device of claim 39 includes in combination a first semiconductor device having a first semiconductor element and ball bumps; and further includes a second semiconductor device having a second semiconductor element, a plurality of terminals, and a resin "covering the main surface of the second semiconductor element and side surfaces of the plurality of terminals, so that a back surface of the second semiconductor element is exposed from the resin, wherein the back and side surfaces of the first semiconductor element are exposed". Applicants respectfully submit that the semiconductor device of claim 39 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The first semiconductor chip 11 in Fig. 1(b) of the Egawa reference is mounted on internal substrate 10 and is encapsulated within resin 13. Accordingly, the Egawa reference as relied upon by the Examiner does not disclose or make obvious a first semiconductor element wherein back and side surfaces thereof are exposed, as featured in claim 39. The structure in Fig. 1(b) of the Egawa reference therefore does not achieve a higher level of heat discharge performance as the semiconductor device of claim 39. Moreover, since the structure in Fig. 1(b) of the Egawa reference includes internal substrate 10 on which the first and second semiconductor chips 11 and 17 are

mounted, the structure in Fig. 1(b) of the Egawa reference cannot achieve a lower profile as the semiconductor device of claim 39 which does not include a base plate.

Fig. 11 of the Imasu et al. reference as relied upon by the Examiner merely discloses semiconductor chip 10 mounted on rigid board 2. Fig. 11 of the Imasu et al. reference as relied upon by the Examiner thus does not disclose a semiconductor device with first and second semiconductor elements and having a low profile, as featured in claim 39. Moreover, since adhesive 16 in Fig. 11 of the Imasu et al. reference covers the surface of semiconductor chip 10 on which external terminals 13 are disposed as well as side surfaces thereof, the structure in Fig. 11 of the Imasu et al. reference does not achieve a higher level of heat discharge performance as the semiconductor device of claim 39. Accordingly, Applicants respectfully submit that the semiconductor device of claim 39 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 39-44, is improper for at least these reasons.

#### **Claims 45-52**

Applicants respectfully submit that claims 45-48, as respectively dependent upon claims 34 and 29, distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner, for at least the reasons as set forth above and by further reason of the features therein.

The semiconductor device of claim 49 includes in combination a first

semiconductor device having a first semiconductor element and ball bumps; and further includes a second semiconductor device having a second semiconductor element, a plurality of terminals, and a resin, "wherein the first semiconductor device has a plurality of conductive material, parts of the conductive material are electrically collected to the ball bumps and other parts of the conductive material are electrically connected to the terminals of the second semiconductor device". Although not necessarily limited thereto, the conductive material of claim 49 may be interpreted as at least readable on terminals 2 in Fig. 9(A) of the present application.

Applicants respectfully submit that the prior art as relied upon by the Examiner does not disclose a semiconductor device including in combination a first semiconductor element having ball bumps located on a back surface thereof, and a second semiconductor element, as featured in claim 49. In Fig. 1(B) of the Egawa reference, bumps 15 are disposed on internal substrate 10, not first semiconductor chip 11. In Fig. 11 of the Imasu et al. reference as relied upon by the Examiner, semiconductor chip 10 is mounted on a rigid board 2, and does not have a second semiconductor element mounted thereto. Also, since the structures in the prior art noted above respectively include an internal substrate and a rigid board, the prior art structures do not achieve a low profile as the semiconductor device of claim 49. Accordingly, Applicants respectfully submit that the semiconductor device of claim 49 distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons.

**Conclusion**

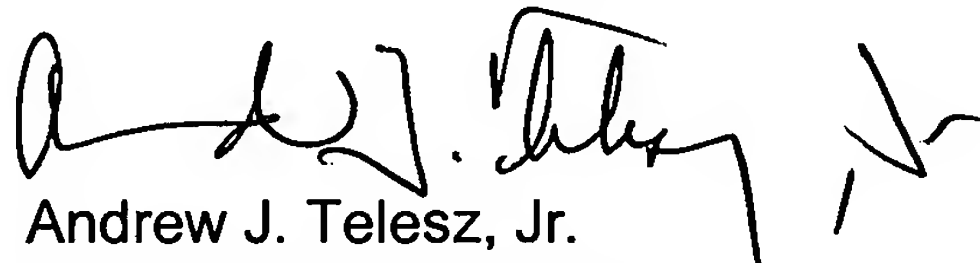
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.

  
Andrew J. Telesz, Jr.  
Registration No. 33,581

One Freedom Square  
11951 Freedom Drive, Suite 1260  
Reston, Virginia 20190  
Telephone No.: (703) 715-0870  
Facsimile No.: (703) 715-0877